Thermal Considerations for QFN Packaged Integrated Circuits

Over the past few years, Quad Flat No-Lead (QFN) packages have become very popular for audio amplifier applications needing efficient power dissipation in small footprints. These packages, shown in Figure 1, are available in a variety of sizes and pin counts. These leadless packages share a common feature, called a thermal flag, on the bottom of the device.

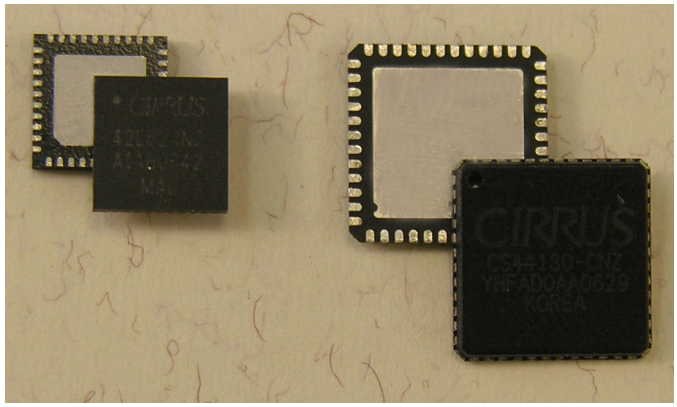


Figure 1. Quad Flat No-Lead QFN Packages

This thermal flag provides a low thermal resistance path which conducts heat out of the device and into whatever structure to which the thermal flag is attached. In most cases, this structure is a printed circuit board (PCB), effectively turning the PCB into a heat sink. Addtionally, some devices use the thermal flag as an electrical connection from the device to the PCB. To ensure optimum performance and system reliability, care must be taken to ensure the QFN device is properly coupled to the PCB structure, both electrically and thermally. Additionally, the system designer must consider how to most effectively transfer the heat away from the device once it conducts into the PCB.

This Application Note will familiarize the system designer with the thermal features of the QFN package, accurately describe the methods and techniques that the system designer should use to achieve optimum thermal performance, and demonstrate the effect of system-level constraints on the thermal performance of the design.

1. THE QFN/PCB THERMAL STRUCTURE

It is helpful to think of the QFN device and the area of the PCB surrounding its footprint as a structure in which heat flows. A cut-away view of the structure is shown in Figure 2.

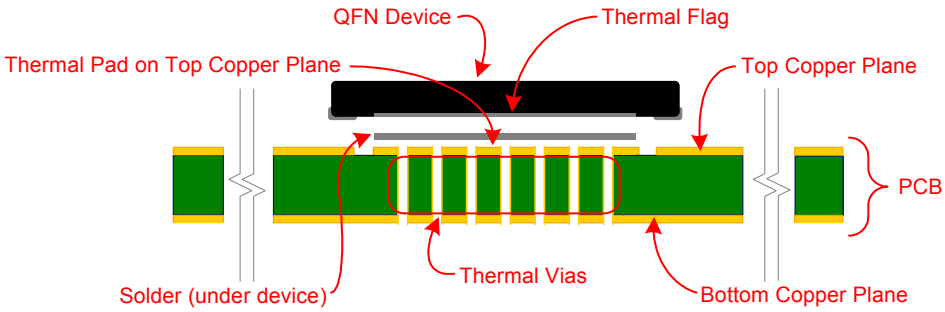


Figure 2. Cut-Away View of a QFN & PCB Structure on a 2-Layer PCB

The structure consists of the QFN device and its thermal flag, a layer of solder between the device and the PCB, a thermal pad created in the top plane of the PCB, a via array under the device, and the PCB structure around the device.

To understand how the elements of the structure work together to conduct heat away from the device, one should visualize the heat traveling throughout the structure as lumped heat conduction paths. A helpful illustration of this basic idea is found in Figure 3. While not technically rigorous, visualizing the system in this manner is effective when considering the flow of heat out of the QFN device and into the surrounding environment.

As can be seen in Figure 3, there are essentially four dominant paths for heat to transfer out of the device into the PCB. The first is indicated by the small light pink arrows on top of the device. These arrows represent the path into the ambient air mass around the device. The dark pink arrows represent the conduction into the PCB through the top plane. The orange arrows extending into the internal copper planes and dielectric material of the PCB represent the heat that travels into the inner board layers through the via array. Finally, the dark red arrows show the heat that travels through the via array under the device and into the PCB's bottom-most copper plane.

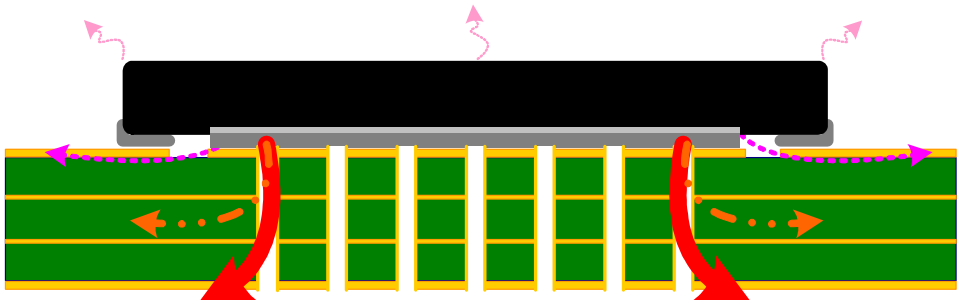


Figure 3. Heat Conduction Paths Away from the Device

2. OPTIMIZING THE THERMAL FLAG INTERFACE

It is important to note that, with the exception of the surface-to-ambient conduction path (shown by the light pink arrows in Figure 3), all of the lumped conduction paths travel through the solder connection between the thermal flag on the device to the thermal pad on the board. For this reason, care must be taken to ensure that the thermal resistance occuring at this interface is as low as possible.

The thermal pad provides a mating surface for the thermal flag on the bottom of the device. The sizing of the thermal pad is straightforward, as it should be made as large as the thermal flag on the bottom of the device. The unlikely exception to this rule is any instance in which making the thermal pad this size would violate the minimum clearances found through the use of the IPC-7351 standard.

In order to efficiently transfer heat from the thermal flag to the thermal pad, there must be a sufficient amount of solder in place at the interface between them. However, too much solder will compromise the reliability of the design, as excess solder can cause bridging between the thermal pad under the device and the signal pins on the perimeter of the device.

Through experimental methods, it has been shown that the area of solder paste applied to the thermal pad should be approximately 50 to 80% of the area of the thermal pad. For instance, a thermal pad measuring 7 mm x 7 mm has an area of 49 mm^2. The area of solder paste applied to this thermal pad should be between 24.5 mm^2 and 39.2 mm^2.

When the solder paste becomes liquid during the soldering process, it releases gas in a process called out-gassing. Uncontrolled out-gassing can cause reliability problems by creating solder voids and bridges underneath the device. To allow the solder to out-gas in a more controlled manner, the solder should be applied in multiple smaller sections instead of in one large section. This is easily accomplished by creating an array of openings in the solder stencil for the thermal pad. Please see Figure 4 for an illustration of this practice when using a 7 mm x 7 mm thermal pad. This method can be scaled to thermal pads of various sizes by changing both the number and the size of the stencil apertures.

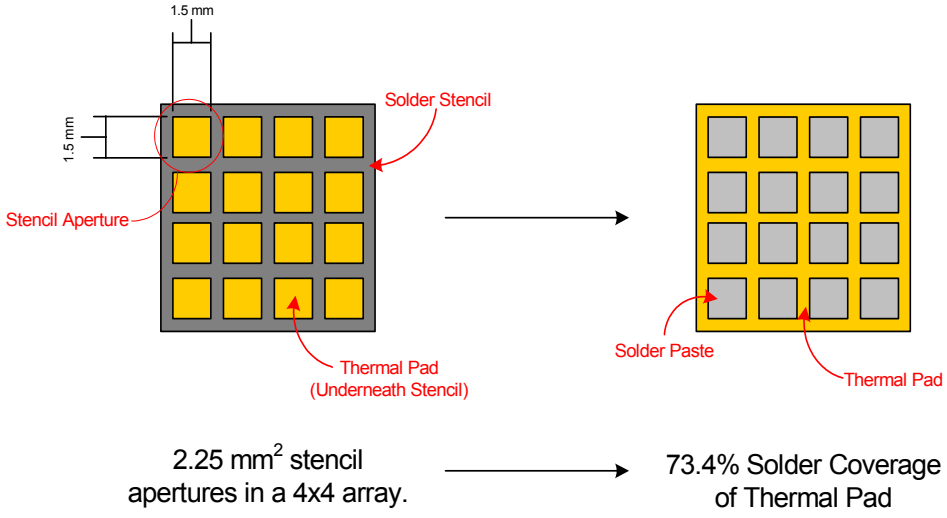


Figure 4. Solder Stencil Apertures for 7 mm x 7 mm Thermal Pad and 73.4% Solder Paste Coverage

3. OPTIMIZING THE CONDUCTION PATH INTO THE TOP LAYER

The conduction of the heat from the device into the top layer of the board is shown by the dark pink arrows in Figure 3. This conduction path is compromised by the copper voids created by the signal traces going into the device and the passive components that are required to be close to the device. The system designer can improve the thermal conductivity of the region surrounding the device by filling all unused areas with copper tied to the ground plane. The amount of copper that fills the area between the traces should be limited only by the minimum spacing required by the voltage levels present on the traces. A good example of this technique is shown in Figure 5 (copper fill is shown in green).

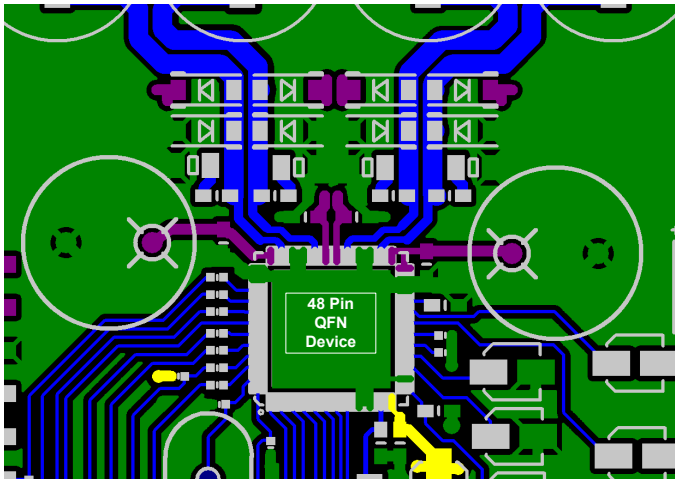


Figure 5. Copper Fill in Unused Areas of the PCB Top Layer

4. OPTIMIZING THE CONDUCTION PATHS THROUGH THE THERMAL VIAS

As shown in Figure 3, the remaining conduction paths (represented by the orange and red arrows) extend from the device and into the rest of the layers (both copper and dielectric) through the thermal vias underneath the device. These conduction paths, if optimized through proper design of the thermal via array, are the most efficient paths in the structure for removing heat from the device.

When considering the design of the thermal via array, it is helpful to first identify an ideal structure for the purpose of heat conduction. After the theoretical ideal is established, the system designer can attempt to design in a more practical structure that will closely replicate the ideal structure.

Figure 6. Ideal Structure under Device for Heat Conduction

With this in mind, the theoretically ideal structure is identified as a solid structure, with very low thermal resistance, such as the copper slug shown in Figure 6. Commonly known as a “heat slug,” this copper slug is viable from a manufacturing standpoint, but is certainly not the most cost-effective solution to implement. A much more cost-effective solution is to create a copper structure within the PCB made from plated vias—a very affordable alternative to the heat slug. This structure is implemented as an array of thermal vias under the device, embedded in the thermal pad of the PCB. An example of a *thermal via array* is shown in Figures 7 and 8.

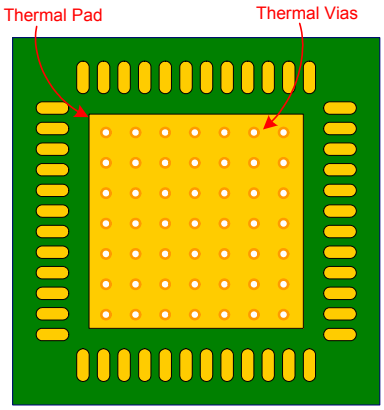


Figure 7. Cost-Effective Array w/Footprint Shown

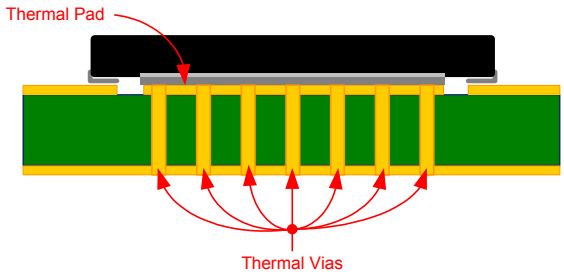


Figure 8. Cost-Effective Thermal Via Array

It is important to note that the thermal vias created should *not* be created with thermal reliefs, such as those shown in Figure 9. These thermal reliefs, often referred to as “wagon wheels” or “webbed lands”, prevent heat travel through the vias and into the surrounding ground plane during the soldering or rework stages of board production. While this may be preferable in the case of standard component pads, transferring heat into the surrounding copper planes is exactly what the system designer is *trying* to accomplish by placing vias in the thermal pad. For this reason, thermal reliefs should never been used in the via array under the device.

Figure 9. Left—Thermal Relief (not recommended) Right—Solid Thermal Via (Recommended)

There are four important design considerations when creating a thermal via array within the thermal pad. These considerations are number, size, fill material, and the effect of the thermal vias on the thermal interface between the device and the thermal pad.

1. Via Number and Size

The number and size of the vias are limited by the size of the thermal pad and the capabilities of the PCB manufacturer, making their design relatively straightforward. For reliability in the manufacturing process, the drill diameter of the vias should be no less than .25 mm, and the center-line of the vias should remain .9 mm away from the edge of the thermal pad and from each other. It would seem that, since the purpose of adding this via structure is to replicate a solid copper slug, the system designer should add as many vias as possible. However, a law of diminishing returns makes the addition of a large numbers of vias somewhat unnecessary. This is shown in Figure 10. This data was gathered through thermal simulations modeling a 7 x 7 mm device dissipating 3 W of heat into the center of a 580 mm^2 square 4-layer PCB. A good practice is to size the via array to be the same as the dimensions (in mm) of the thermal flag. For instance, a 7 x 7 mm thermal flag would require a 7 x 7 via array; a 5 x 5 mm thermal flag would require a 5 x 5 via array, and so forth.

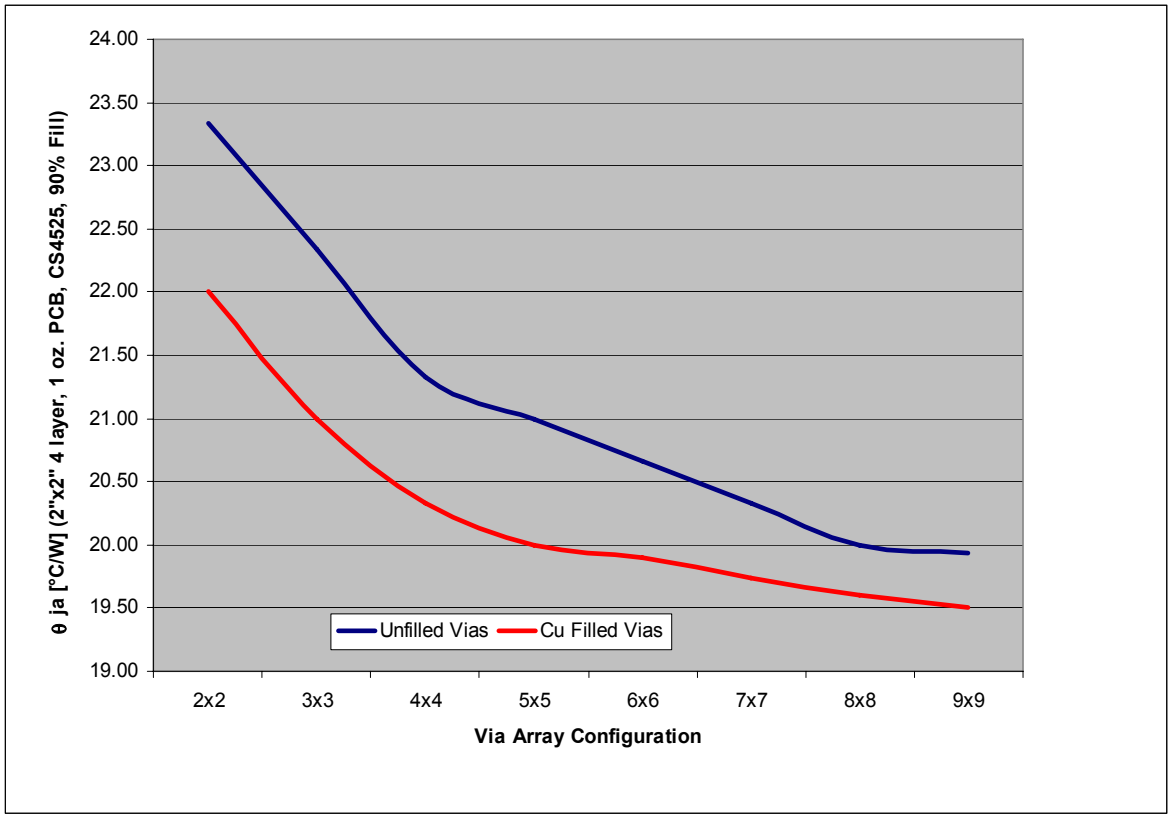


Figure 10. Effect of Number of Vias on PCB Thermal Resistance (θ ja)
Modeled using 4 layer 2" x 2" PCB, dissipating 3W in the 7 x 7mm device.

2. Via Fill Material

Returning again to the theoretically ideal structure, copper would obviously be the preferred fill material for the via. While it is possible to fill the vias with copper (or any one of a number of thermally conductive materials available), the cost increase associated with this process can be unacceptable for cost-sensitive designs. Additionally, filled vias have been found to yield only modest performance gains for applications in which the power dissipated in the device is less than 5 W. This is shown in Figure 10 above.

If thermally conductive fill material is not a viable option for the design, the vias can be optimized by specifying the thickness of the copper covering the internal walls of the via. If this specification is not directly called out in the specification drawing for the PCB, the thermal conductivity of the via may be compromised by having a thin internal wall. It is only necessary to specify a minimum wall thickness, as anything over this thickness will only improve the thermal conductivity of the via. A good starting point is to specify a 1 oz. copper wall thickness, which should result in no cost increase to the design since this is a common practice. Increasing the inner wall thickness beyond this minimum requirement should be decided based upon the manufacturing capabilities of the PCB manufacturer.

3. Effect on the Thermal Interface

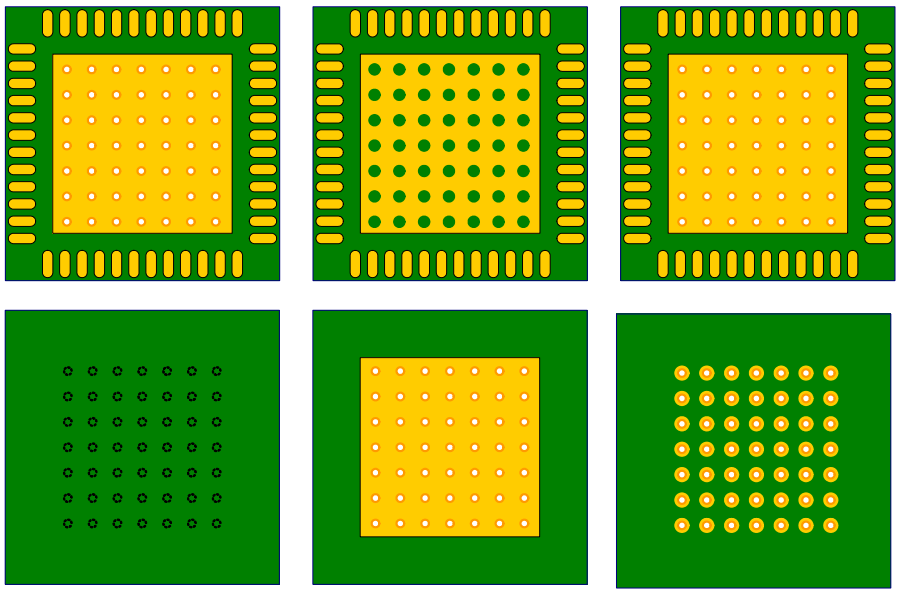
Unfortunately, thermal vias create holes in the PCB. During the the manufacturing process, liquid solder can flow into these holes and away from the part. This phenomenon, known as "solder wicking", can compromise the thermal performance of the entire design if too much solder travels from underneath the device down into the vias.

Figure 11. Solder Voiding Due to Solder Wicking

As shown in Figure 11, solder voids underneath the device (shown in red) increase the thermal resistance of the thermal interface. While filling the vias with copper or thermally conductive epoxy will prevent solder wicking, doing so increases the cost of the PCB. However, there are steps that can be taken to limit the amount of solder wicking that occurs in a design with unfilled vias.

The first step in controlling solder wicking is to maintain a via diameter smaller than .3 mm. When using smaller vias, the surface tension of the liquid solder inside the vias is more capable of countering the force of gravity on the solder within the via. If the via structure is constructed following the guidelines mentioned above, holding the via size to around .25 mm – .3 mm, minimal solder wicking is achieved.

The remaining techniques for limiting solder wicking involve the use of solder mask to restrict the flow of solder from the top side of the PCB to the bottom side. In a process called “tenting”, solder mask is used to prevent solder from either entering or exiting the thermal vias, depending on the side of the board to which the solder mask is placed. In *bottom-side via tenting* (Part A in Figure 12), solder mask is allowed to cover and plug the thermal vias from the bottom side of the PCB, which prevents solder from flowing down the via and onto the bottom of the board. In *top-side via tenting* (Part B in Figure 12), small areas of solder mask are placed over the thermal vias on the top side of the PCB to prevent solder from flowing into the vias from the top side of the board. This method is generally accepted as the better of the two tenting practices since bottom-side via tenting has been shown to increase the size of solder voiding under the device due to outgassing that occurs in the solder that is allowed to flow down into the vias.



A. Bottom Side via Tenting **B. Top Side via Tenting** **C. Via Encroaching**

Figure 12. Techniques to Prevent Solder Wicking (Top and Bottom Vias of Thermal Array Shown)

Via encroaching (Part C in Figure 12) is a technique that is often adopted due to concerns about the presence of solder mask material under the device. This technique allows solder to flow down the via, but restricts the migration of the solder across the bottom plane of the board. This method allows for a small diameter of exposed copper around each of the thermal vias. The exposed copper should be approximately .2 mm larger than the via drill diameter. While effective for limiting excessive solder voiding under the device, the small bumps that are created on the bottom side of the board may cause problems during bottom-side solder paste application for double-sided PCBs. Additionally, in applications that use a heat sink attached to the bottom side of the board to increase thermal performance of the device, the presence of these bumps will prevent good surface contact between the heat sink and the PCB.

5. OPTIMIZING HEAT FLOW AWAY FROM THE DEVICE

With the structure under the device optimized, heat can travel out of the device and into the lower layers of the PCB very efficiently. The ability of the lower layers of the PCB to continue to pull heat away from the device and release it into the ambient air is dictated by the PCB construction. The number of layers used, the weight of the copper, and the placement of signal traces and components are very important in determining how well the lower layers perform as a heat sink.

The important thing to remember concerning heat flow through the PCB and into the ambient air is that the thermal resistance between the heat source and the cooler outer regions of the PCB must be kept as low as possible. This is similar to an electrical circuit where the temperature difference between the device and the cooler regions of the board is represented by a voltage difference. The spreading resistance of the copper planes can be represented by an electrical resistance and the heat flow by an electrical current. This is shown in Figure 13. In the same way an unregulated power supply would “sag” under a very low resistance load, the temperature will begin to sag if the thermal resistances attached between it and a low thermal potential are very low. Contrary to the case of an electrical circuit, a sag in the source is a good thing!

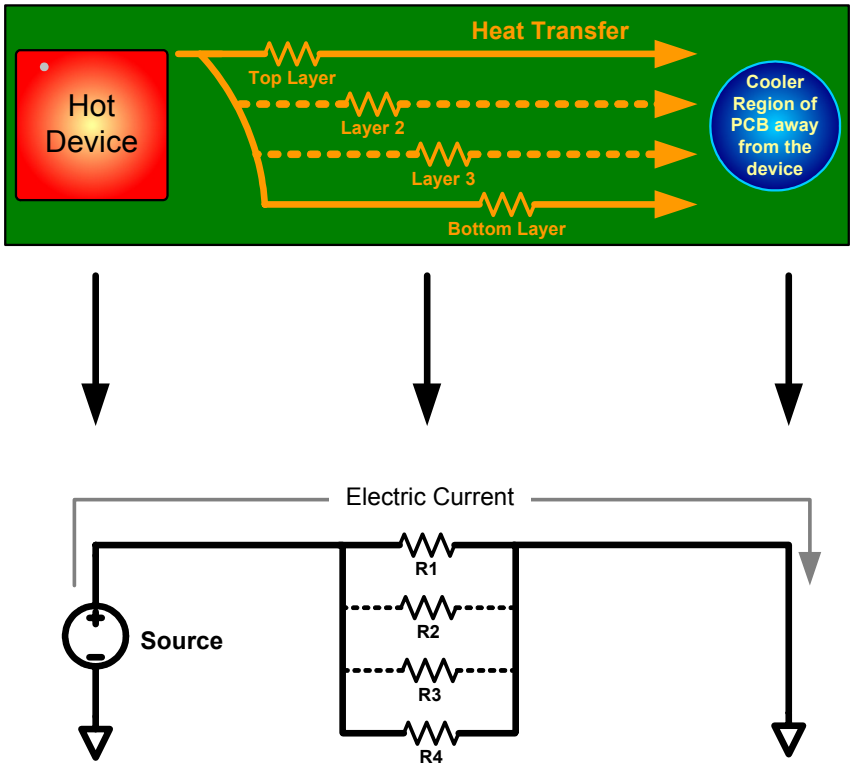


Figure 13. Silimarities between Heat Transfer in a PCB and Electrical Current

In the circuit example, the current flow through the circuit can be increased by one of two methods—either increasing the number of resistors or decreasing the individual resistances of R1 - R4. Likewise, the flow of heat away from the device can be increased by increasing the number of layers or decreasing the thermal resistance of each of the individual layers.

1. Effect of Increasing the Number of Copper Layers

The number of layers in a PCB has a very large impact on how well heat conducts away from the device. While it is probable that the layer count of a design will be chosen for reasons other than thermal mass, this consideration should not be overlooked by the system designer. The effect of adding additional layers of copper can be seen in Figure 14. This thermal model was created to predict the performance of a 7 x 7 mm device in both a 2-layer and 4-layer design, given a minimum board area of 508 mm^2 with 1 oz. copper.

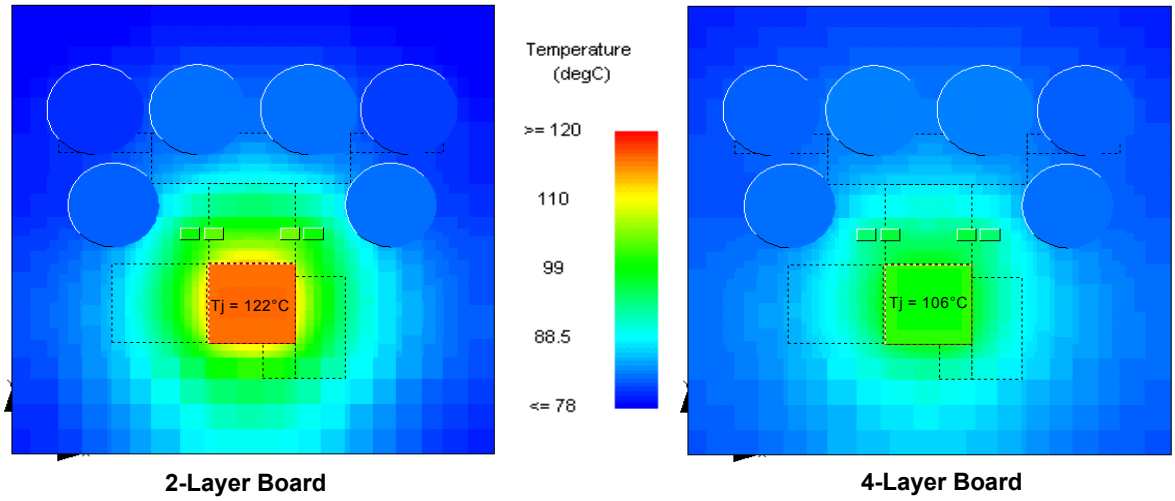


Figure 14. Effect of PCB Layer Count on Heat Dissipation

As can been seen from the plot, the device dissipating 3 W of power into the 2-layer board operates at a temperature nearly 20° C hotter than the same device dissipating the same amount of power into 4-layer board! The thermal contour indicates that the heating in the 2-layer design is much more localized to the device. However, in the 4-layer design, the heat continues to progress towards the edges of the board. This is due to the parallel combination of the spreading resistance of the individual copper layers

2. Effect of Increasing the Thickness of the Copper Layers

One way the system designer can decrease the resistance of each of the layers is by increasing the copper weight of the layers. For cost-sensitive designs, increasing the copper weight provides an opportunity to get more thermal margin without having to incur the costs of additional board layers. As is the case with the number of thermal vias used under the device, there is a law of diminishing returns for increasing copper weight. However, even a small change in copper weight has a large impact on the thermal performance of the PCB.

The impact higher copper weight has on the spreading resistance is readily seen in Figure 15. These plots show the effects of higher spreading resistance on the designs with lower copper weight. Because the heat cannot spread out into the copper, it stays centralized around the device and the region of copper immediately around the device, causing the operating temperature of the device to go up. Additionally, because the heat stays centralized to the device and the immediate region around the device, it heats up a smaller portion of the copper planes, which means there is less “hot” surface area in contact with the cooler ambient air. Just as in the electrical circuit example, there must be a potential difference between a source and a sink in order for heat to flow. If the heat is unable to travel to the outer regions of the PCB, there is very little potential difference between those regions of the PCB and the ambient air. Because of that, heat flow between the source (the outer regions of the PCB) and the sink (the ambient air) is minimal, and the PCB’s capability as a heat sink is restricted to the small region directly around the device.

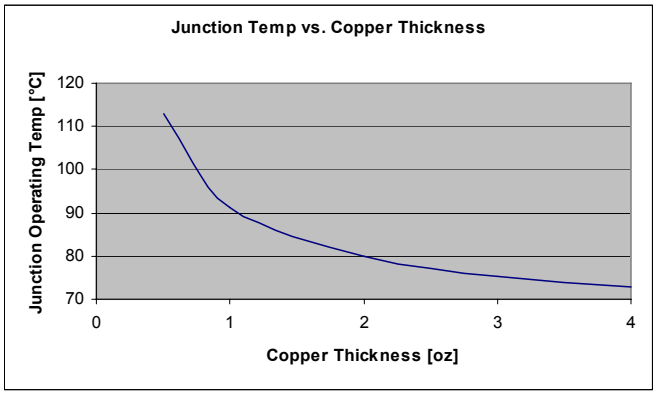


Figure 15a: Law of diminishing returns for copper thickness

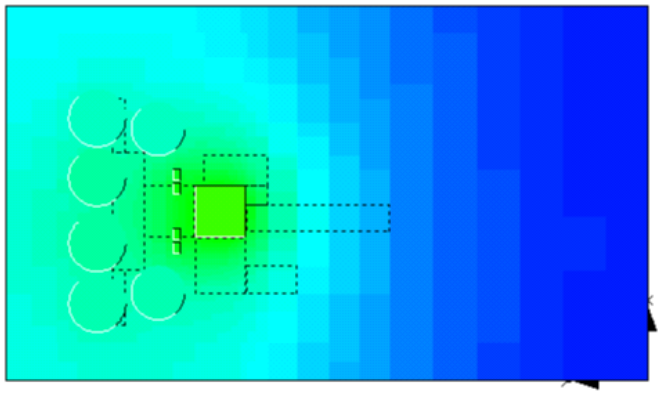


Figure 15d: 7 x 7 mm QFN, 4 Layer, 2 Oz Copper, P_{diss} = 3.5 W

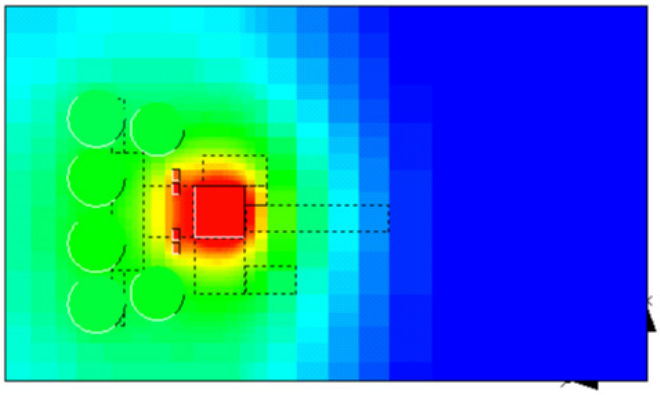


Figure 15b: 7 x 7 mm QFN, 4 Layer, ½ Oz Copper, P_{diss} = 3.5 W

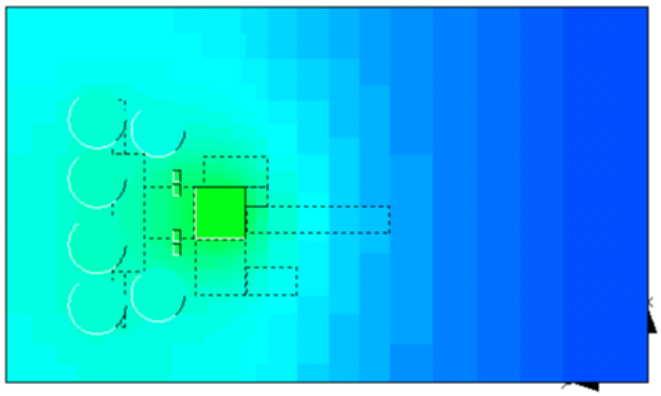


Figure 15e: 7 x 7 mm QFN, 4 Layer, 3 Oz Copper, P_{diss} = 3.5 W

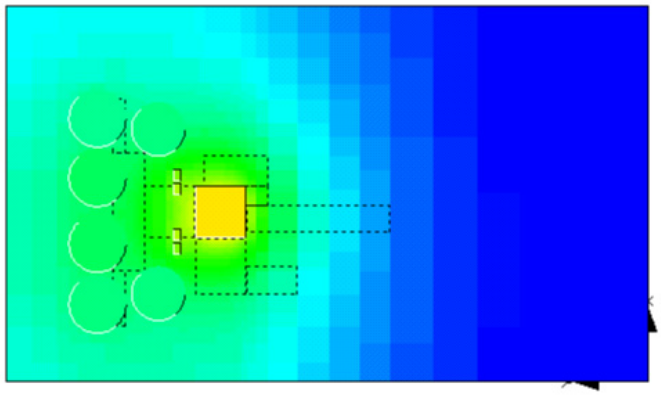


Figure 15c: 7 x 7 mm QFN, 4 Layer, 1 Oz Copper, P_{diss} = 3.5 W

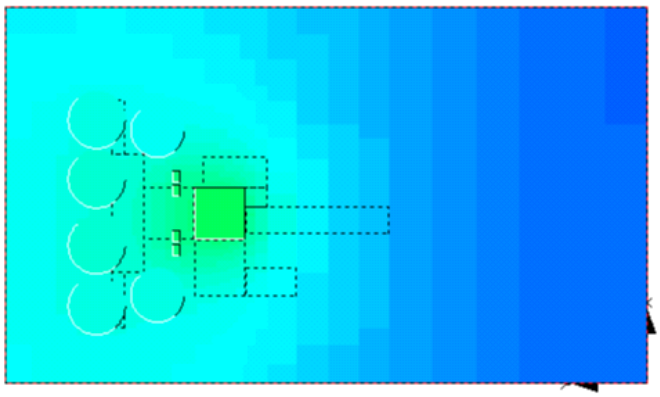


Figure 15f: 7 x 7 mm QFN, 4 Layer, 4 Oz Copper, P_{diss} = 3.5 W

Figure 15. Effect of Copper Thickness on Thermal Performance

3. How Traces Affect the Thermal Resistance of a Copper Layer

As mentioned previously, the top layer heat conduction is limited by the device pins, the traces terminating to those pins, and the passive components surrounding the device. However, on the lower layers of the PCB, the system designer has greater control over the routing of the traces. In order to maximize the thermal performance of the device and PCB structure, the system designer should keep traces on the lower layers of the PCB as far away from the device as possible. This ensures that the solid area of copper under the device is as large as possible for maximum heat conduction away from the part. An illustration of this point is found in Figure 16.

- The first trace, marked number 1, runs parallel to the device. As heat flows out of the device, it encounters a large thermal resistance created by the trace cutting across the copper plane.
- The second trace configuration is better-than the first because it is as far away from the thermal via array as possible. This ensures that heat conduction is only limited by the inherent spreading resistance of the copper layer itself.
- Finally, if it is not possible to avoid having traces close to the device, the third routing method can be used to limit the impact of the traces on heat conduction. Traces running perpendicular to the center of the device present a smaller cross-sectional profile of thermal resistance to heat conducting away from the device.

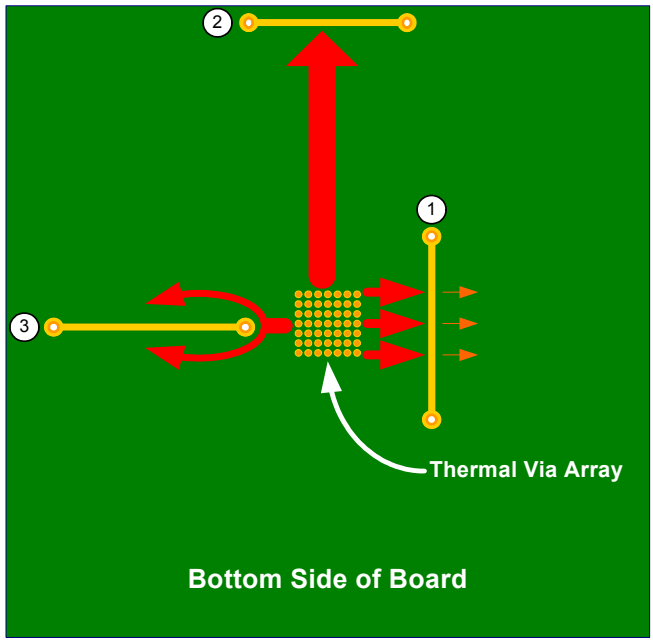


Figure 16. Options for Routing Traces on Lower PCB Layers

The simulation results shown in Figure 17 show that having a trace cut across the copper plane, as in option 1 above, causes a significant rise in operating temperature when compared to having the trace far away from the device, as in option 2. The operating temperature of the device was very similar between options 2 and 3, confirming that if bottom-side traces must be near the device, running them perpendicular to the device is a reasonable option.

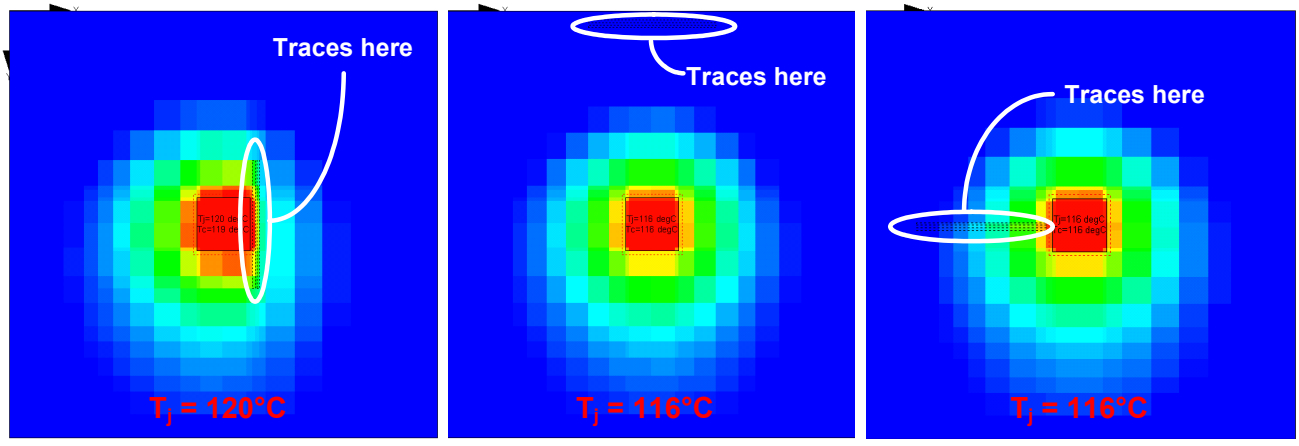


Figure 17. Effect of Trace Location and Directions on Heat Conduction within the Lower PCB Layers

6. REFERENCES

1. *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame® (MLF®) Packages*, Amkor Technology, Inc., Revision E, December 2003.
2. IPC Standards for PCB Design standard 7351-*Generic Requirements for Surface Mount Design and Land Pattern Standard*, Association Connecting Electronics Industries (IPC), Bannockburn, IL 60015.

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